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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,915	02/08/2001	Kazuyuki Kikuchi	401071	5831

23548 7590 11/29/2004

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EXAMINER	
GARBOWSKI, LEIGH M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/778,915	KIKUCHI, KAZUYUKI	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,17,20 and 23-26* is/are rejected.

7)☒ Claim(s) *18,19,21,22,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

Claim 20 is objected to because of the following informalities: "circuits" [line 2] should be singular for proper antecedent basis.

Claim 26 is objected to because of the following informalities: "circuit" [line 14] should be plural for proper antecedent basis; "arranged the same order" [line 17]; and the claim must end in a period. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

What is meant by "and from two sides of the first packaged integrated circuit that are respectively adjacent to the facing side of the first packaged integrated circuit" [lines 4-7] claim is not clear. How two sides can be respectively adjacent to the facing side is confusing.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16-17, 20, 23, 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Murasawa et al. [U.S. Patent #5,309,020].

As per claim 16, a semiconductor device structure comprising: a substrate; a first packaged IC including a package and having a plurality of terminals extending outwardly from a periphery of the package, the first packaged IC being mounted on the substrate; a second packaged IC including a package and having a plurality of terminals

extending outwardly from a periphery of the package, the second packaged IC being mounted on the substrate, wherein at least some of the terminals of the first packaged IC are connected to corresponding terminals of the second IC, and the terminals of the first and second packaged ICs that are connected to each other are arranged facing each other on the substrate whereby the first and second packaged ICs are compactly mounted on the substrate [figure 1; SUMMARY OF THE INVENTION; column 3, lines 8-12, 16-24, 31-38, 56-58]. As per claim 17, wherein the packages of the first and second packaged ICs have respective sides from which the respective terminals that are connected to each other project and the respective sides of the first and second packaged ICs face each other [column 4, lines 17-19]. As per claim 20, wherein the terminals of the first packaged IC that are connected to the terminals of the second packaged IC are arranged in a group, in series, the terminals of the second packaged IC that are connected to the terminals of the first packaged IC are arranged in a group, in series, and the terminals of the first packaged IC are arranged in the same order as the terminals of the second packaged IC [column 3, lines 31-47]. As per claim 23, wherein the first and the second packaged ICs are mounted on the same side of the substrate [figure 1]. As per claim 25, wherein the packages of each of the first and second packaged ICs have respective facing sides, the facing sides of the first and second packaged ICs face each other, and the terminals of the first packaged IC project from the facing said of the first packaged IC [figure 1].

Claims 16-17, 20, 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Papageorge et al. [U.S. Patent #5,438,224].

As per claim 16, a semiconductor device structure comprising: a substrate; a first packaged IC including a package and having a plurality of terminals extending outwardly from a periphery of the package, the first packaged IC being mounted on the substrate; a second packaged IC including a package and having a plurality of terminals extending outwardly from a periphery of the package, the second packaged IC being mounted on the substrate, wherein at least some of the terminals of the first packaged IC are connected to corresponding terminals of the second IC, and the terminals of the first and second packaged ICs that are connected to each other are arranged facing

each other on the substrate whereby the first and second packaged ICs are compactly mounted on the substrate [figures 1 and 7; SUMMARY OF THE INVENTION; column 4, lines 16-28]. As per claim 17, wherein the packages of the first and second packaged ICs have respective sides from which the respective terminals that are connected to each other project and the respective sides of the first and second packaged ICs face each other [figure 1; column 2, line 60]. As per claim 20, wherein the terminals of the first packaged IC that are connected to the terminals of the second packaged IC are arranged in a group, in series, the terminals of the second packaged IC that are connected to the terminals of the first packaged IC are arranged in a group, in series, and the terminals of the first packaged IC are arranged in the same order as the terminals of the second packaged IC [column 4, lines 22-24, 31-33]. As per claim 24, wherein the first and the second packaged ICs are mounted on the opposite sides of the substrate and connections between connected terminals of the first and second packaged ICs pass through respective through-holes in the substrate [column 4, lines 3-6, 36-53]. As per claim 25, wherein the packages of each of the first and second packaged ICs have respective facing sides, the facing sides of the first and second packaged ICs face each other, and the terminals of the first packaged IC project from the facing said of the first packaged IC [column 2, line 60; column 22-24, 31-33].

As per claim 26, a semiconductor device structure comprising: a substrate; a first packaged IC including a rectangular package having a pair of longer sides and a pair of shorter sides and having a plurality of terminals extending outwardly from the longer sides of the package, the first packaged IC being mounted on the substrate; and a second packaged IC including a rectangular package having a pair of longer sides and a pair of shorter sides and having a plurality of terminals extending outwardly from the longer sides of the package, the second packaged IC being mounted on the substrate, wherein at least some of the terminals of the first packaged IC, as a first group of terminals, are connected to corresponding terminals of a second group of terminals of the second IC, shorter sides of each of the first and second packaged ICs face each other, and the first group of terminals and the second group of terminals are arranged in series, the terminals of the first and second groups closest to the shorter sides of the

packages of the first and second packaged ICs that face each other are connected to each other [figure 1; SUMMARY OF THE INVENTION; column 4, lines 16-28].

Claims 16-17, 20, 23-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Mori et al. [U.S. Patent #5,834,843].

As per claim 16, a semiconductor device structure comprising: a substrate; a first packaged IC including a package and having a plurality of terminals extending outwardly from a periphery of the package, the first packaged IC being mounted on the substrate; a second packaged IC including a package and having a plurality of terminals extending outwardly from a periphery of the package, the second packaged IC being mounted on the substrate, wherein at least some of the terminals of the first packaged IC are connected to corresponding terminals of the second IC, and the terminals of the first and second packaged ICs that are connected to each other are arranged facing each other on the substrate whereby the first and second packaged ICs are compactly mounted on the substrate [figure 3 and 4 and 7A; column 4, lines 25-43; column 5, lines 15-18; column 6, lines 40-41]. As per claim 17, wherein the packages of the first and second packaged ICs have respective sides from which the respective terminals that are connected to each other project and the respective sides of the first and second packaged ICs face each other [figures 3 and 4]. As per claim 20, wherein the terminals of the first packaged IC that are connected to the terminals of the second packaged IC are arranged in a group, in series, the terminals of the second packaged IC that are connected to the terminals of the first packaged IC are arranged in a group, in series, and the terminals of the first packaged IC are arranged in the same order as the terminals of the second packaged IC [column 5, liens 28-34]. As per claim 23, wherein the first and the second packaged ICs are mounted on the same side of the substrate [figure 7A]. As per claim 24, wherein the first and the second packaged ICs are mounted on the opposite sides of the substrate and connections between connected terminals of the first and second packaged ICs pass through respective through-holes in the substrate [figures 8A and 11A; column 7, line 13; column 8, lines 40-41, 45-53]. As per claim 25, wherein the packages of each of the first and second packaged ICs have respective facing sides, the facing sides of the first and second packaged ICs face each

other, and the terminals of the first packaged IC project from the facing said of the first packaged IC [figures 3 and 4].

As per claim 26, a semiconductor device structure comprising: a substrate; a first packaged IC including a rectangular package having a pair of longer sides and a pair of shorter sides and having a plurality of terminals extending outwardly from the longer sides of the package, the first packaged IC being mounted on the substrate; and a second packaged IC including a rectangular package having a pair of longer sides and a pair of shorter sides and having a plurality of terminals extending outwardly from the longer sides of the package, the second packaged IC being mounted on the substrate, wherein at least some of the terminals of the first packaged IC, as a first group of terminals, are connected to corresponding terminals of a second group of terminals of the second IC, shorter sides of each of the first and second packaged ICs face each other, and the first group of terminals and the second group of terminals are arranged in series, the terminals of the first and second groups closest to the shorter sides of the packages of the first and second packaged ICs that face each other are connected to each other [figure 3 and 4 and 7A; column 4, lines 25-43; column 5, lines 15-18, 28-34; column 6, lines 40-41].

Allowable Subject Matter

Claims 18-19, 21-22, 27-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

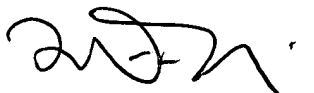
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from examiner Andrea Liu should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LEIGH M. GARBOWSKI
PRIMARY EXAMINER